

REMARKS

Claims 1-55 stand rejected. Claim 52 has been amended. Reconsideration of the application in view of the amendments and remarks set forth below is respectfully requested.

Rejections Under 35 U.S.C. § 102

The Examiner rejected claims 1-10, 12-21, 23-31, 35-41, 43-50, and 52-55 under 35 U.S.C. § 102(b) as being anticipated by Vivio (U.S. Pat. No. 5,706,447). With regard to independent claims 1 and 13, the Examiner stated:

Vivio discloses a method of switching control of a bus in a processor-based device, the method comprising the acts of:

- Electrically coupling a first bus controller to the bus (col. 4., lines 18-36)
- Generating a detection signal indicative of coupling of a second bus controller to the bus; and (col. 4, lines 18-12)
- Automatically isolating the first bus controller from the bus in response to the detection signal (col. 4, lines 18-62)

Independent claims 21, 23, 35, 44, 51, and 52 were rejected on similar grounds.

Applicants respectfully traverse these rejections for at least two reasons discussed in further detail below. First, the Vivio reference does not disclose switching control of a bus. Second, the Vivio reference does not disclose isolating a first bus controller from a bus in response to the detection of a signal indicating the coupling of a second bus controller to the bus.

Anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under Section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15

U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under Section 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

Applicants respectfully submit that the Examiner does not fully appreciate certain features recited in the present claims. As stated by Applicants in their response to the previous official action, the present application is directed to a system and method of automatically switching control of a bus in a processor-based device. Pg. 2, lines 7-8. While certain system motherboards may include a controller for controlling devices on a bus, such as a SCSI controller for controlling SCSI devices, many end-users may desire incorporation of alternate controller cards which provide different or additional features. Pg. 3, line 21-Pg. 4, line 2. Accordingly, in one exemplary embodiment, to enable a user to install an alternative controller on an expansion card via an I/O port, the locally resident bus controller is coupled to a switch/terminator module to automatically switch control of the bus and the devices on the bus from the locally resident bus controller to a bus controller on an expansion card whenever an expansion card is connected to the expansion port. Pg. 8, line 20 - Pg. 9, lines 1-4. When an expansion card is connected to the system motherboard, the locally resident bus controller is isolated from the bus such that a controller on the expansion card assumes control of the bus and the devices on the bus. Pg. 10, lines 1-3.

The independent claims 1, 13, 21, 23, 35, 44, 52, and 53 of the present application recite a method or device for either 1) automatically isolating a first bus controller from the bus, in response to a second bus controller being coupled to the bus (or in response to the generation of a detection signal indicating that a second controller has been coupled to the

bus), or 2) switching control of a bus from a first controller to a second controller. Based on the similarity of the Examiner's rejections with respect to each of the independent claims, these points will be discussed together. While the specific recitations may vary with regard to one or more specific independent claims, the discussion below may be applicable to each of the independent claims.

The Vivio reference clearly does not disclose either switching control of a bus or isolating a first bus controller from the bus, as recited in the pending claims. In contrast, the Vivio reference discloses "a system for automatically maintaining proper bus termination." Abstract, lines 1-2. As stated in the Description of the Related Art section of the Vivio reference:

it is desirable for the P6 processors to be located at the ends of the bus for signal quality reasons....However, this type of architecture creates difficulties for maintaining proper bus termination [because in the]...case where no module is plugged into a connector at one end of the bus, termination must be provided on the PCB motherboard [but in the]...case where a processor is plugged into the connector at one end of the bus, the effective end of the bus changes [from the PCB motherboard] to be located on the processor module. Thus to maintain proper termination, the termination on the motherboard must be removed, and the bus must be terminated at the effective bus end on the processor module. Col. 3, lines 6-24.

In order to address the problem set forth above, Vivio discloses a system that permits the bus termination point to switch from the motherboard to the processor module. Col. 4, lines 27-36. Specifically, looking to Fig. 5 of Vivio, when the processor module 542 is inserted into the connector 210, the terminator 224 is switched off by the switching device 222. This allows the terminator 548, which is located on the processor module 542, to become the termination point for that side of the bus. Col. 8, lines 50-66. If the processor module 542 is removed from

the connector 210, the switching device 222 is switched on, and the terminator 224 once again becomes the termination point for that side of the bus. Col. 8, line 63 – col. 9, line 4.

The Vivio reference simply *does not* disclose switching control of a bus from a first bus controller to a second bus controller, as recited in the present claims. There is virtually no discussion in the Vivio reference regarding control of the computer bus 120, and there is no discussion in the Vivio reference regarding switching control of computer bus 120 from one bus controller to another. In fact, the Vivio reference only uses the words “bus” and “control” in the same sentence once, and that use is clearly unrelated to bus control as it involves interrupt control devices. *See* col. 5, lines 62-67.

Further, the Vivio reference also *does not* disclose automatically isolating a first bus controller from the bus in response to a second bus controller being coupled to the bus (and/or in response to a detection signal indicating that a second bus controller has been coupled to the bus), as recited in each of the independent claims. Indeed, as described above, the Vivio reference merely discloses a switching device 222 that permits the termination point on one side of a bus to shift from the terminator 224 to the terminator 548 when the processor module 542 is coupled to the connector 210. This is clearly in contrast to the subject matter recited in the present claims. Accordingly for this further reason, the Vivio reference cannot possibly anticipate the subject matter recited in the present claims.

For at least the reasons set forth above, it is clear that the present claims recite elements that are not disclosed in the Vivio reference. Accordingly, the subject matter recited in independent claims 1, 13, 21, 23, 35, 44, 52, and 53, as well as those claims dependent thereon, cannot possibly be anticipated by the Vivio reference. As such, Applicants

respectfully request withdrawal of the Examiner's rejections under 35 U.S.C. § 102 (e) and allowance of claims 1-10, 12-21, 23-33, and 35-55.

Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 11, 22, and 34 under 35 U.S.C. § 103(a) as being unpatentable over Vivio (U.S. Patent No. 5,706,447) in view of Applicant's Admitted Prior Art ("AAPA") and claims 32-34, 42, and 51 under 35 U.S.C. § 103(a) as being unpatentable over Vivio (U.S. Patent No. 5,706,447) in view of Gasparik et al. (U.S. Patent No. 6,072,943).

The Examiner rejected claims 11, 22, and 34 under 35 U.S.C. § 103 (a) as being unpatentable over Vivio in view of Applicant's Admitted Prior Art ("AAPA"). The rejected claims each depend from independent claims which, for the reasons set forth above, include subject matter which is not disclosed by the Vivio reference. Applicants respectfully submit that the AAPA does nothing to cure the deficiencies discussed above with respect to the Vivio reference. Accordingly, Applicants submit that claims 11, 22, and 34 cannot be rendered obvious by the cited combination and respectfully request withdrawal of the rejection of claims 11, 22, and 34 under 35 U.S.C. § 103 (a).

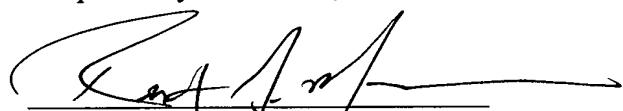
The Examiner rejected claims 32-34, 42, and 51 under 35 U.S.C. § 103(a) as being unpatentable over Vivio (U.S. Patent No. 5,706,447) in view of the Gasparik reference. The rejected claims each depend from independent claims which, for the reasons set forth above, include subject matter which is not disclosed by the Vivio reference. Applicants respectfully submit that the Gasparik reference does nothing to cure the deficiencies discussed above with respect to the Vivio reference. Specifically,

because the Gasparik reference only discloses a single bus controller circuit 190, it *cannot possibly* cure the deficiencies in the Vivio reference that were outlined above. Accordingly, Applicants assert that claims 32-34, 42, and 51 cannot be rendered obvious by the cited combination and respectfully request withdrawal of the rejection of claims 32-34, 42, and 51 under 35 U.S.C. § 103 (a).

Conclusion

In view of the remarks set forth above, Applicants respectfully request allowance of claims 1-55. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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